CLAIMS

WHAT IS CLAIMED IS:

1. A method of manufacturing an integrated circuit having trench isolation regions in a substrate including a first layer, the method comprising:

selectively etching the first layer to form apertures associated with locations of the trench isolation regions;

forming strained semiconductor material above the first layer; and

forming insulative material in the apertures to form the trench isolation regions.

2. The method of claim 1, wherein the strained semiconductor material is formed on sidewalls of the apertures.

3. The method of claim 1, wherein strained semiconductor material is formed after the insulative material is formed.

4. The method of claim 1, wherein the strained semiconductor material is formed before the insulative material is formed.

5. The method of claim 3, wherein the strained semiconductor material is formed by selective epitaxial growth.

6. The method of claim 1, further comprising:

siliciding the strained semiconductor material.

7. The method of claim 1, wherein the strained semiconductor material is silicon and the first layer is silicon-germanium.

8. The method of claim 1, wherein the first layer is above a BOX layer.

9. A method of forming shallow trench isolation structures in a compound semiconductor layer above a buried oxide (BOX) layer, the method comprising:

providing a hard mask layer above the compound semiconductor layer;

removing the hard mask layer at locations;

forming trenches in the compound semiconductor layer under the locations;

stripping the hard mask layer;

forming a strained semiconductor layer above the compound semiconductor layer; and

providing isolation material in the trenches to form the shallow trench isolation structures.

10. The method of claim 9, further comprising providing a silicide layer above the strained semiconductor layer.

11. The method of claim 10, wherein the strained semiconductor layer is provided by selective silicon epitaxial growth.

12. The method of claim 9, wherein the isolation material is provided by deposition.

13. The method of claim 12, further comprising providing a liner in the trenches at low temperature.

14. The method of claim 13, wherein the low temperature is below 750°C.

15. The method of claim 14, wherein the liner is silicon dioxide grown in an oxygen-containing atmosphere.

16. The method of claim 9, wherein the trenches have a bottom reaching the BOX layer.

17. An integrated circuit, comprising:

a compound semiconductor layer;

a buried oxide (BOX) layer beneath the compound semiconductor layer;

a strained semiconductor layer above the compound semiconductor layer; and

isolation trenches disposed in the compound semiconductor layer, wherein the isolation trenches include insulative material and sidewalls, the sidewalls of the isolation trenches are at least partially covered by the strained semiconductor layer.

18. The integrated circuit of claim 17, further comprising a gate structure between the isolation trenches.

19. The integrated circuit of claim 18, wherein the strained semiconductor layer is silicided at a location of a source and a drain.

20. The integrated circuit of claim 17, wherein the strained semiconductor material is silicon and the compound semiconductor material is silicon-germanium and the trenches extend from the strained semiconductor material at a top to the buried oxide layer at a bottom.